PATENT ABSTRACTS OF JAPAN

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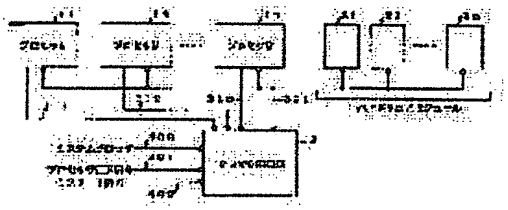
(54) DEBUGGING BACK-UP DEVICE FOR MULTIPROCESSOR SYSTEM

(57)Abstract:
PURPOSE: To grasp the internal states of all processors constructing a multiprocessor system and all hard modules at the time of a break point of the processor to be debugged.
CONSTITUTION: The processors 11-1n are connected to each other and work synchronously with a system clock 301, and the hardware modules 21-2m are also connected to each other and work synchronously with the clock 301. The processors 11-1n output the stop signals 311-31n at the time of their break points, respectively. A clock control part 3 usually outputs a system clock 400 as it is as the clock 30 and stops the clock 301 when a stop signal is inputted from a debugging subject processor designated by a processor selection signal 401. Then, the clock 301 is started again with application of a restart signal 402.



LEGAL STATUS

[Date of request for examination]

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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] While two or more processor and two or more hardware modules transmit data mutually, with respect to the debugging exchange equipment of the multiprocessor system which performs processing in juxtaposition, especially, this invention can clarify a processor and relation of operation between both hardware modules, and relates to the debugging exchange equipment of a multiprocessor system which enabled it to debug the whole multiprocessor system easily.
[0002]
[Description of the Prior Art] Generally, debugging of a program inserts the break point into the program, stops activation of a processor for this every break point, and is performed by observing the situation of the processor at that time. On the other hand, with the multiprocessor system, the high performance system is built by carrying out parallel processing, arranging two or more processor and two or more hardware modules, and transmitting data mutually.
[0003] As a technique which supports the debugging activity of such a multiprocessor system conventionally, the approach of making grasp of the program state of all processors easy at the time of a halt of the processor for debugging is learned by stopping other processors with the stop signal from the processor which reached the break point as indicated by JP,63-85942,A, for example.
[0004]
[Problem(s) to be Solved by the Invention] In the above-mentioned conventional technique, since it was not taking into consideration about stopping other hardware modules which are operating synchronizing with each processor at the time of a break point, the internal state of other hardware modules in the halt time of each processor has not been grasped, but system-wide debugging was difficult.
[0005] The purpose of this invention is to offer the debugging exchange equipment which becomes possible [grasping the internal state of all other hardware modules] in the program of all the processors that constitute the multiprocessor system in the halt time of the processor used as the candidate for debugging and an internal state, and a list.
[0006]
[Means for Solving the Problem] The debugging exchange equipment of the multiprocessor system concerning this invention Two or more processors which operated synchronizing with the system clock and were connected mutually, To the system which consists of two or more hardware modules which similarly operated synchronizing with the system clock and were connected to mutual [said / two or more processors and mutual] When a stop signal is inputted from one or more processors which serve as a candidate for debugging among said two or more processors These system clocks to said all processor and said all hardware modules including the processor concerned are stopped, and it has a clock control means to resume a system clock with the restart signal from the outside.
[0007]
[Function] A user can specify one or more processors used as the candidate for debugging. When all these all [any one or] for debugging reach a break point and they send out a stop signal, a clock control means stops a system clock by the break of the machine cycle of a processor etc., and makes coincidence suspend actuation of all system-wide components. The situation of operation in a system

can be correctly observed by reading the contents of the register of other hardware modules etc. to the memory of all the processors at the time of this halt, the contents of the register, and a list. Then, if a system clock is resumed with the restart signal from the outside, actuation of a system can be continued normally and efficient trace and debugging of all the components of a multiprocessor system will be attained.

[0008]

[Example] Hereafter, a drawing explains one example of this invention to a detail.

[0009] Two or more processors 11-1n which drawing 1 is the block diagram showing the 1st example which applied this invention, operated synchronizing with the system clock 301, and were connected mutually, Two or more hardware modules 21-2m which similarly operated synchronizing with the system clock 301, and were connected to mutual [said / two or more processors 11-1n and mutual], The stop signals 311-31n from each processors 11-1n and the processor selection signal 401 from the outside, and the restart signal 402 perform halt/restart control of a system clock 400. It consists of the clock control sections 3 which output a system clock 301 to each processors 11-1n and each hardware modules 21-2m.

[0010] If each processors 11-1n reach a break point, they will output stop signals 311-31n. Although the clock control section 3 usually supplies the system clock 400 from the outside to the whole system as a system clock 301 through, if the stop signal from the processor specified with the processor selection signal 401 which shows the processor for debugging among the stop signals 311-31n from each processors 11-1n is inputted, it will suspend the output of a system clock 301. Thereby, actuation of all Processors 11-1n and hardware modules [21-2m] system components stops to coincidence. Therefore, all the situations of operation in a multiprocessor system can be correctly observed by reading all processors [at the time of this halt / 11-1n] memory, the contents of the register, the contents of the hardware modules [besides a list / 21-2m] register, etc. Then, if the restart signal 402 is made more active than the exterior, the clock control section 3 will supply a system clock 400 to the whole system as a system clock 301 through again, and will resume actuation of a system.

[0011] Drawing 2 shows the example of a concrete configuration of the clock control section 3 in drawing 1 . the processor selection signal 401 for a decoder 41 to specify the processor for debugging given from the outside in drawing -- decoding -- output signals 411-41n -- at least one is activated. The output signals 411-41n of a decoder 41 and the stop signals 311-31n from Processors 11-1n are inputted into AND circuits 51-5n, respectively. If the stop signal in the AND circuit which became active [the output signal of a decoder 41] among these AND circuits 51-5n becomes active (i.e., if the stop signal of the processor specified with the processor selection signal 401 becomes active), a flip-flop 42 will change to a set condition through OR circuit 50. Usually, although a flip-flop 42 is in a reset condition and the system clock 400 is then outputted as a system clock 301 as it is through AND circuit 30, if it will be in a set condition, AND circuit 30 will be closed and will stop a system clock 301. Then, if the restart signal 402 is made more active than the exterior, a flip-flop 42 will return to a reset condition, AND circuit 30 will open it, and a system clock 400 will be again outputted as a system clock 301 through AND circuit 30.

[0012] In addition, when the processor used as the candidate for debugging is plurality, two or more output signals [of a decoder 41 / 411-41n] things are chosen. In this case, it is at the generating time of the stop signal which became active most early among the corresponding stop signals from two or more processors, a flip-flop 42 will be in a set condition, and the output of a system clock 301 will stop.

[0013] Drawing 3 is the block diagram of other examples of the part 6 enclosed with the broken line in drawing 2 , and when all of the stop signal of two or more processors for debugging become a bitter taste tape, it is an example in the case of stopping a system clock. In drawing 3 , a decoder 41 activates output signals other than the processor for debugging specified with the processor selection signal 401 among output signals 411-41n. When the output signals 411-41n of a decoder 41 and the stop signals 311-31n from Processors 11-1n are inputted into OR circuits 61-6n, respectively and all the stop signals from the processor for debugging specified with the processor selection signal 401 become active, all OR circuits [61-6n] outputs become active, consequently the output of AND circuit 60 becomes active, and the set condition of the flip-flop 42 of drawing 2 will be satisfied.

[0014] Drawing 4 shows a hardware modules [in drawing 1 / 21-2m] example. (a) of drawing 4 is the example of a configuration of a FIF0 buffer module, connects two or more registers (here seven pieces) to concatenation, and consists of a shift control register 212 which controls the shift action of FIF0 buffer 211 which shifts the input data from a data input line to this entry sequence one by one to a data output line side, and this FIF0 buffer 211 synchronizing with a system clock 301. Moreover, (b) of drawing 4 is the example of a configuration of a timer module, and when the value of the data register 221 with which presetting of the data showing the appointed time of day is carried out, the counter 222 which counts time of day synchronizing with a system clock 301, and a data register 221 is compared with the counted value of a counter 222 and both are in agreement, it consists of a gate circuit 224 for taking the timing of the comparator circuit 223 which outputs the appointed time-of-day report signal, and the presetting to a data register 221.
[0015] Drawing 5 is the block diagram showing the 2nd example which applied this invention, and synchronizes with a system clock 301. And synchronizing with a system clock 301, it operates as well as two or more processors 11-1n connected to mutual [which operates by the machine cycle of a round term]. Two or more hardware modules 21-2m connected to mutual [said / two or more processors 11-1n and mutual], With the stop signals 311-31n and the processor selection signal 401 from the outside, the restart signal 402, and the machine cycle signal 403 from each processors 11-1n Halt/restart control of a system clock 400 is performed, and it consists of the clock control sections 3 which output a system clock 301 to each processors 11-1n and each hardware modules 21-2m.
[0016] If each processors 11-1n reach a break point, they will output stop signals 311-31n. Although the clock control section 3 usually supplies the system clock 400 to the whole system as a system clock 301 through, if the stop signal from the processor for [which was specified with the processor selection signal 401 among the stop signals 311-31n from each processors 11-1n] debugging is inputted, it will suspend the output of a system clock 301 at the ending point of the machine cycle under activation. Thereby, since Processors 11-1n and all hardware modules [21-2m] system components stop to coincidence, all the situations of operation in this multiprocessor system in the termination time of a machine cycle can be correctly observed by reading the contents of the other hardware modules [21-2m] register etc. to all processors [at the time of this halt / 11-1n] memory, the contents of the register, and a list. Then, if the restart signal 402 is made more active than the exterior, the clock control section 3 will be again supplied to the whole system by making a system clock 400 into a system clock 301 synchronizing with the initiation time of a machine cycle, and will resume actuation of a system.
[0017] According to the configuration of drawing 5 , since a halt/restart of the system clock in the instruction unit of the program of a processor can carry out correctly, the more efficient trace of it is attained.
[0018] Drawing 6 shows the example of a concrete configuration of the clock control section 3 in drawing 5 . In drawing 6 , actuation of the part enclosed with the broken line shown by 6 is the same as that of the same part of drawing 2 . That is, if the stop signal from the processor for [which was specified with the processor selection signal 401 among each processors / 11-1n / stop signals] debugging becomes active, a flip-flop 42 will change to a set condition through OR circuit 50. In addition, this broken-line part 6 can also be replaced by drawing 3 . In this case, a flip-flop 42 will change to a set condition on the conditions from which all the stop signals from two or more processors for [which was specified with the processor selection signal 401] debugging became active.
[0019] If the above-mentioned flip-flop 42 will be in a set condition, the output signal 420 will become active. The machine cycle synchronization circuit 43 will set an output signal 430 to 0 synchronizing with the machine cycle signal 403, if the output signal 420 of a flip-flop 42 becomes active as shown in drawing 7 . If the output signal 430 of the machine cycle synchronization circuit 43 is set to 0, AND circuit 30 will close and a system clock 301 will be stopped. Then, if the restart signal 402 is activated, as a flip-flop 42 shows a reset condition at return and drawing 7 , the output signal 430 of the machine cycle synchronization circuit 43 will be set to 1 synchronizing with the machine cycle signal 403, and a system clock 301 will resume.
[0020]
[Effect of the Invention]

(1) Since the whole system including a processor and the other hardware module can be suspended to coincidence by specifying the processor from which a user becomes a candidate for debugging according to the break point of an object processor according to claim 1, the situation of operation in a system can be correctly observed by reading the contents of other hardware modules etc. to the memory of all the processors at the time of a halt, the contents of the register, and a list. Furthermore, actuation of a system can be normally continued with the restart signal from [from this halt point in time] the outside, and it can greatly contribute to easy-ization of efficient trace of all the components of a multiprocessor system, and a debugging activity.

[0021] (2) According to claim 2, since a system clock can be stopped by the break of the machine cycle of a processor, a halt/restart of actuation in the instruction unit of the program of a processor can be carried out, and exact trace is attained.

[0022] (3) Efficient trace is attained even if it inserts many break points into a program, since a system clock can be stopped by the break point of the beginning of the processors used as the candidate for debugging according to claim 3.

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CLAIMS

[Claim(s)]
[Claim 1] Debugging exchange equipment of the multiprocessor system which comes to provide a clock control means for two or more processor and two or more hardware modules to be connected mutually respectively, to be debugging exchange equipment of the multiprocessor system which operates synchronizing with a system clock, to stop the system clocks to said all processors and said hardware modules including the processor concerned if a stop signal is inputted from one or more processors for debugging, and to resume this system clock with the restart signal from the outside.
[Claim 2] It is debugging exchange equipment of the multiprocessor system according to claim 1 characterized by for said two or more processors operating by the machine cycle of the same period, and being said clock control means at the termination time of the machine cycle under activation, stopping said system clock ignited by said stop signal from the processor used as said candidate for debugging, and resuming said system clock with the restart signal from the outside synchronizing with the initiation time of a machine cycle.
[Claim 3] Said clock control means is claim 1 characterized by stopping said system clock at the input time of said stop signal of the beginning of the processors used as said candidate for debugging, or debugging exchange equipment of a multiprocessor system given in two.

[Translation done.]

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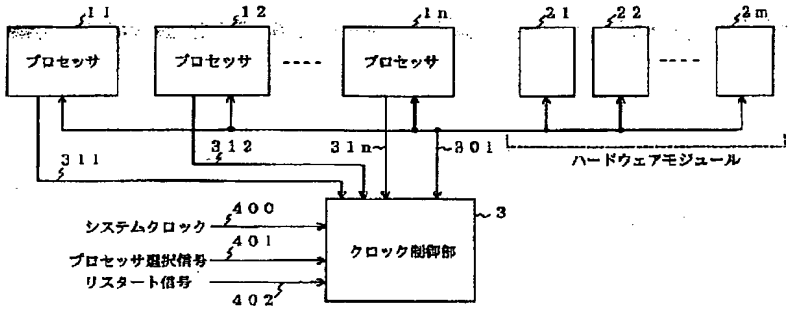
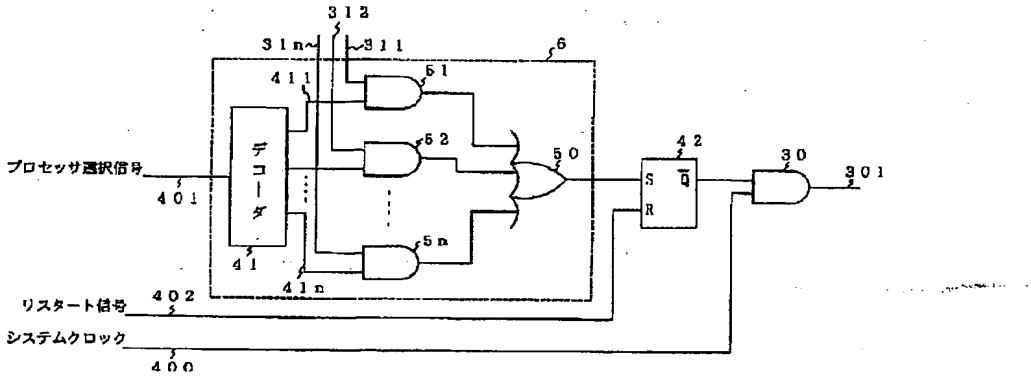
DRAWINGS

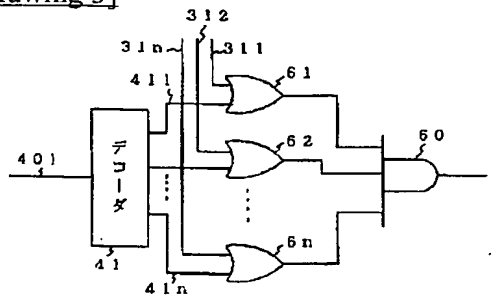
[Drawing 1]



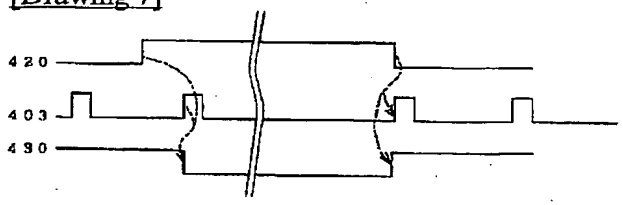
[Drawing 2]



[Drawing 3]

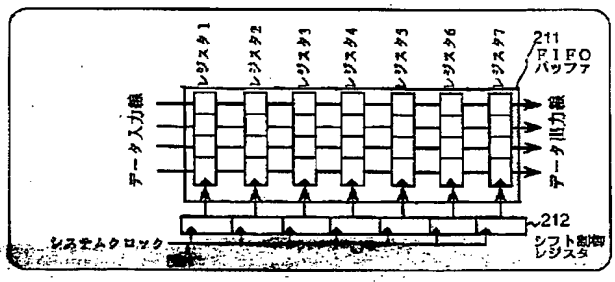


[Drawing 7]

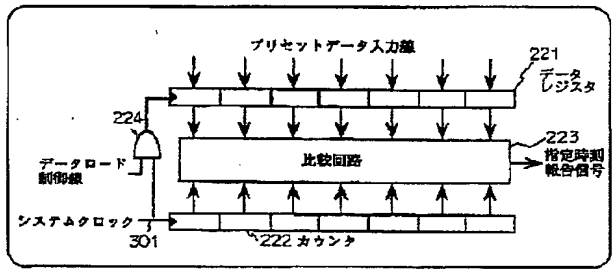


[Drawing 4]

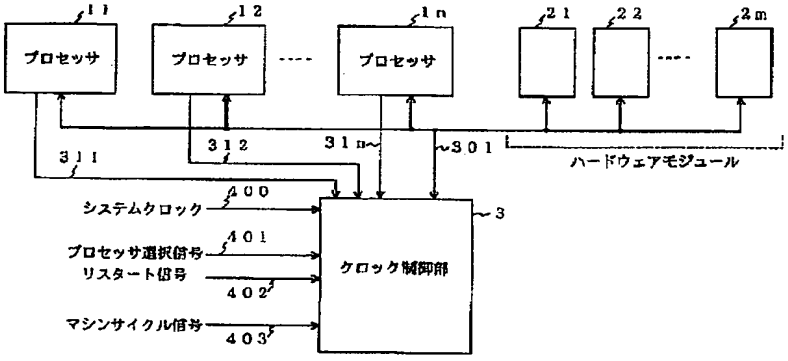
(a) FIFOバッファモジュール



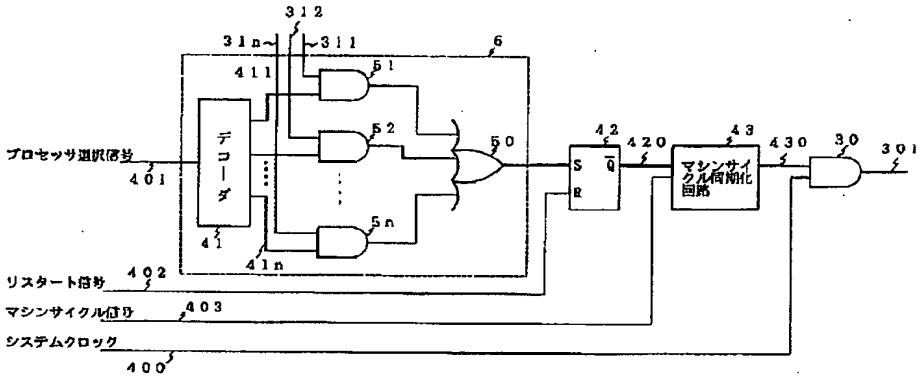
(b) タイマモジュール



[Drawing 5]



[Drawing 6]



[Translation done.]

IBM Technical Disclosure Bulletin Vol. 37 No. 04B April 1994

Checkstop-on-Stop Capability for Multiprocessor Debug

This article describes a multiprocessor debug technique that enables any processor in the system, when stopped, to stop all other processors, thus providing a useful tool for hardware and software debug in a multiprocessor environment.

A multiprocessor system containing processors that have no means of receiving and responding to the stopped condition of another processor in the system can hinder hardware and software debug. Debug can be hindered because it isn't possible to observe the state of all processors immediately following a condition that caused one processor to stop, such as an instruction address compare (breakpoint). Ideally, a processor could signal all other processors that it has stopped, and in turn, each processor would stop. Some processors, for example, provide a function whereby prior to stopping, the processor sends a quiesce request to the system, and waits for a "system quiesced" response back from the system. This technique allows the system chips to respond to the stopped condition of the processor, but it can't necessarily be used to stop other processors in the system, because the processors may not have a quiesce request input pin, and may be unaware that the system is stopping.

The checkstop-on-stop technique allows any processor, upon stopping, to checkstop all other processors in the system. The state of each processor can then be examined. To implement this, the system can provide a switch, that, when activated, allows a stopped condition reported by any of the processors to signal a checkstop to the system, stopping the other processors.

A checkstop is similar to a hard stop in that the processor is stopped immediately, but can't be restarted from the point at which it was stopped. A soft stop, on the other hand, allows the processor to quiesce by running additional cycles, and allows the processor to be restarted from the point where it was stopped. If the processor doesn't provide an input pin for soft stop, a checkstop provides the best method for stopping the processor via a hardware signal.

Checkstop-on-stop improves the debug capabilities of a multiprocessor system, while requiring a minimal amount of hardware. Debug capabilities are improved by enabling observation of each processor's state immediately following a stopped condition reported by any processor.

INTERNATIONAL SEARCH REPORT

Int. nal Application No
PCT/IL 03/00671

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F11/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 193 187 A (SPIX GEORGE A ET AL) 9 March 1993 (1993-03-09) column 1, line 29 - line 35 column 2, line 50 -column 3, line 33 column 4, line 36 -column 5, line 21 column 5, line 39 - line 50 column 6, line 10 - line 20 figures 2,3,5,7,11	1-8
X	US 5 678 003 A (BROOKS JEFFREY S) 14 October 1997 (1997-10-14) column 2, line 26 - line 54 column 3, line 18 - line 62 column 5, line 55 - line 65 column 6, line 4 - line 51 figures 1,3,4	1-8

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 February 2004	10/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Rinelli, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte[illegible] al Application No
PCT/IL 03/00671

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 132 (P-1704), 4 March 1994 (1994-03-04) & JP 05 313946 A (NIPPON TELEGR & TELEPH CORP ;OTHERS: 02), 26 November 1993 (1993-11-26)	1,5
A	abstract	2,6
X	"CHECKSTOP-ON-STOP CAPABILITY FOR MULTIPROCESSOR DEBUG" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 37, no. 4B, 1 April 1994 (1994-04-01), page 455 XP000451312 ISSN: 0018-8689 abstract	1-8